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A Noble Research on Low Power Explicit Pulse Triggered Flip Flop Design Based on a Signal Feed-Through Scheme

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ABSTRACT

In this brief, Pulse-triggered FF (P-FF) is a single-latch structure which is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the advantages of speed, its circuit simplicity lowers the power consumption of the clock tree system The low-power flip-flop (FF) design featuring an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is presented. This proposed P-FF design successfully solves the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance. Based on post-layout simulation results using TSMC CMOS 90-nm technology, this proposed P-FF design outperforms the conventional P-FF design by using only 24 transistors. The average power delay of flip flop is reduced up to 3.57 µW.

Index Terms—Flip-flop (FF), low power, pulse triggered flip flop (P-FF)

I. INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry. The needs for low power have created a major paradigm shift where power dissipation has become as important a consideration as performance and area. So this Low Power P-FF reviews various strategies and methodologies for designing low power circuits and systems. It specify the many issues facing designers at architectural, circuit, logic and device levels and presents some of the techniques that have been proposed to overcome these difficulties. This article concludes with the future challenges that must be met to design the low power, high performance of systems.

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In digital designs system now a day's ever adopt intensive pipelining techniques and required many flip flop rich modules such as shift register, register file and first in-first out. It's also estimated that the power consumption of the clock system, which is consists of clock distribution networks and storage elements, it's as high as 50% of total system power. Flip flops thus contribute a significant portion of the chip area and power consumption to the overall system design.

A P-FF consists of a pulse generator (PG) for strobe signals and a latch for data storage. If triggering pulses are sufficiently narrow, then latch acts like an edge-triggered flip flop. Since only one latch has been opposed to two in the conventional master–slave configuration, is needed, a pulse trigger FF is simpler in circuit complexity. This will be leads to a higher toggle rate for high speed operations. Pulse triggered flip flops also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Even with these advantages, pulse generation (PG) circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. In this statistical design framework is developed to take these factors into account. To obtain the accurate balanced performance among power, area and delay design space exploration is also a widely used technique.

In this brief, we present a novel approach to low-power pulse trigger FF design based on a signal feed-through scheme. To observing the delay discrepancy in latching data 0 and 1, the design manages to shorten the longer delay by using feeding the input signal directly to an internal node of the latch design to speed up the data transition. This type of significant mechanism is implemented by introducing a simple pass transistor for extra signal driving. When it combined with the PG circuitry, it forms a new pulse trigger FF design with enhanced speed and power-delay-product (PDP) performances.

II. CONVENTIONAL P-FF DESIGNS

P-FFs, in terms of pulse generation (PG), can be classified as an explicit or an implicit type FF. In an implicit type pulse trigger-FF, the PG is part of the latch design and no explicit pulse signals are generated. In an explicit type pulse trigger flip flop, the pulse generator and the latch are both separate. Without generating pulse signals explicitly, implicit type pulse trigger FFs is in general more power economical. However, they are suffering from a longer discharging path problem, which leads to inferior timing characteristics. Explicit pulse generation, on a adverse, incurs more power consumption but the logic separation from latch design gives the FF design a unique speed advantage. Its power consumption as well as the circuit complexity can be effectively reduced if one pulse generator is shares with a group of FFs (e.g., an n-bit register). In this brief design, thus we will focus only on the explicit type P-FF designs.

A. EP-DCO: explicit -Data closed to output Flip-Flop

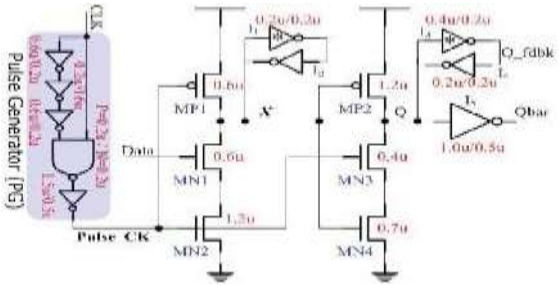


Fig.2.1(a) ep-DCO

To provide a comparison, some existing pulse triggered flip flop designs are reviewed first. Fig. 2.1(a) shows a classic explicit pulse trigger flip flop design that has named data-closet-to-output (ep-DCO). It consists of a NAND-logic-based pulse generator (PG) and a semi-dynamic true single-phase-clock (TSPC) structured latch design. In this pulse triggered flip flop design, inverters I3 and I4 are used to a latch data, and inverters I1 and inverter I2 are used to hold internal node of X. The pulse width of ep-DCO is determined by the delay of three inverters. But this design suffers from a serious drawback, i.e., the internal node X of ep-DCO is discharged on every rising edge of the clock in spite of the presence of a static input "1". This problem gives rise to large switching power dissipation. To overcome this drawback, many remedial measures such as conditional capture, conditional discharge, conditional precharge, and conditional pulse enhancement scheme has been proposed.

B. CDFF: conditional discharged Flip- Flop:

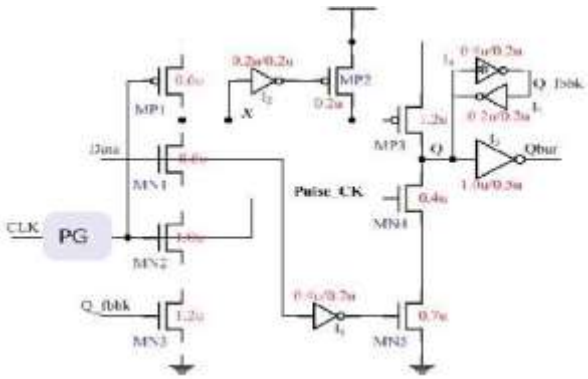


Fig.2.1(b)CDFF

Fig. 2.1(b) shows a conditional discharged (CD) technique .An extra n-MOS transistor MN3 controlled by the output signal Q-feedback is employed so that no discharge occurs if the input data remains "1." In addition, the

keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up pMOS transistor only.

C. SCDFF: Static- conditional discharged Flip-Flop:

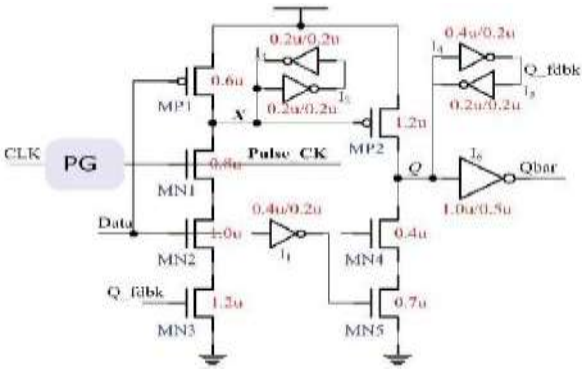


Fig.2.1(c) SCDFF

Fig. 2.1(c) shows a similar P-FF design using a static conditional discharge (SCDFF) technique. Its differs from the CDFF design in using of a static latch structure. The node 'X' is exempted from periodical pre- charges. It exhibits a longer data-to-Q (D to Q) delay than the CDFF design. Both designs are face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1, MN2 and MN3. To overcome this delay problem for better speed performance, a powerful pull-down circuitry has been needed, which has causes extra layout area and power consumption of flip flop. The modified hybrid-latch flip-flop (MHLFF).

D. MHLFF: Modified hybrid latch flip-flop:

Fig. 2.1(d) also uses a static latch structure. The keeper logic at node 'X' has been removed. A weak pull up transistor MP1 controlled by the output signal 'Q' maintains the level of node X when 'Q' equals 0. Even with its circuit simplicity, the MHLFF designed contain two drawbacks. First one is since node X is not pre-discharged node, a prolonged 0 to 1 delay has expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT) is applied to the dis-charging transistor MN3. Second, node 'X' becomes floating in certain cases and its value may have drifted causing extra dc power.

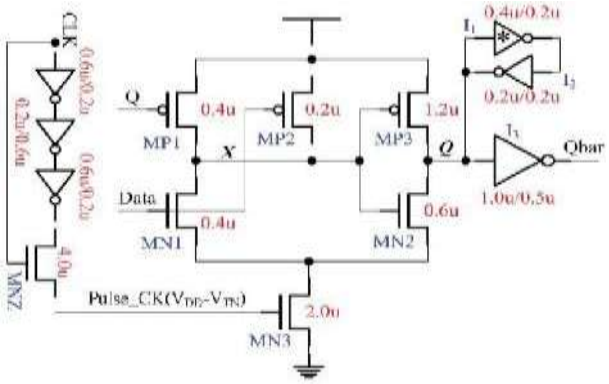


Fig.2.1(d) MHLFF

The proposed design, as shown in Fig. 2.2, accept two measures to overcome the problems associated with existing pulse trigger FF designs. The first one significant is to reducing the number of nMOS transistors stacked in the discharging path of flip flop. The second one solution is supporting a mechanism to conditionally enhance the pull down strength when input data is '1.' Refer to Fig. 2.2, as it opposed to transistor stacking design in Fig.2.1 (a), (b), (c), (d) and (e), this pulse trigger FF design discharging path using PTL. The transistor N2, in conjunction with an additional transistor N3, forms two input pass transistor logic (PTL) based AND gate to control the discharge of transistor N1. Since the two inputs to the AND gate logic are mostly complementary.

III. PROPOSED PULSE TRIGGER FLIP FLOP DESIGNS:

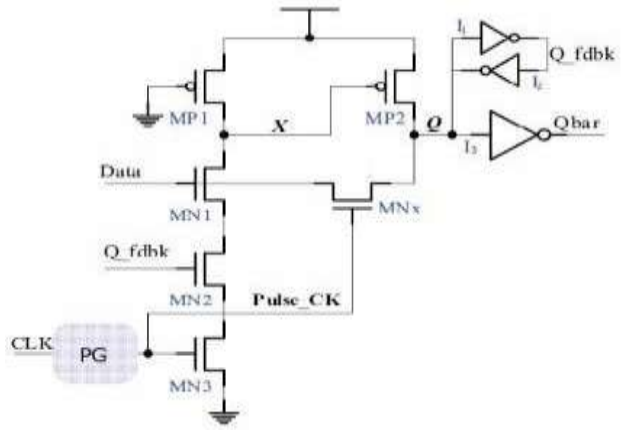


Fig.3.1 proposed P-FF design

Recalling the circuits reviewed in implicit and explicit, they all removed the same worst case timing occurring at 0 to 1 data transitions. Referring to Figure 3.1, the proposed design adopts a signal feed-through technique to improve this delay. Conditional discharge scheme to avoid unnecessary switching at an internal node. However, there are three Similar to the SCDFF design, the proposed flip flop design also employs a static latch structure and a major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one

1. A weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This will be gives rise to a pseudo-nMOS logic style design and the charge keep circuit for the internal node X can saved. In addition to circuit simplicity, this approach will also reduce the load capacitance of node X.

2. A pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates signal driving from the input source to node Q. The node level can be quickly pulled up to shorten the data transition delay of flip flop.

3. The pull-down network of the second stage inverter is completely removed.
Instead, the newly employed pass transistor MNx provides a discharging path of flip flop. The role played by pass transistor (MNx) is thus dual, i.e. it providing extra driving to a node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. This scheme actually improves the "0" to "1" delay and thus reduces the discrepancy between the rise time and the fall time delays. In comparison with other pulse trigger FF designs such as EP- DCO, CDFF, SCDFF and MHLFF, the proposed design shows the most balanced delay behaviors.

IV. RESULTS

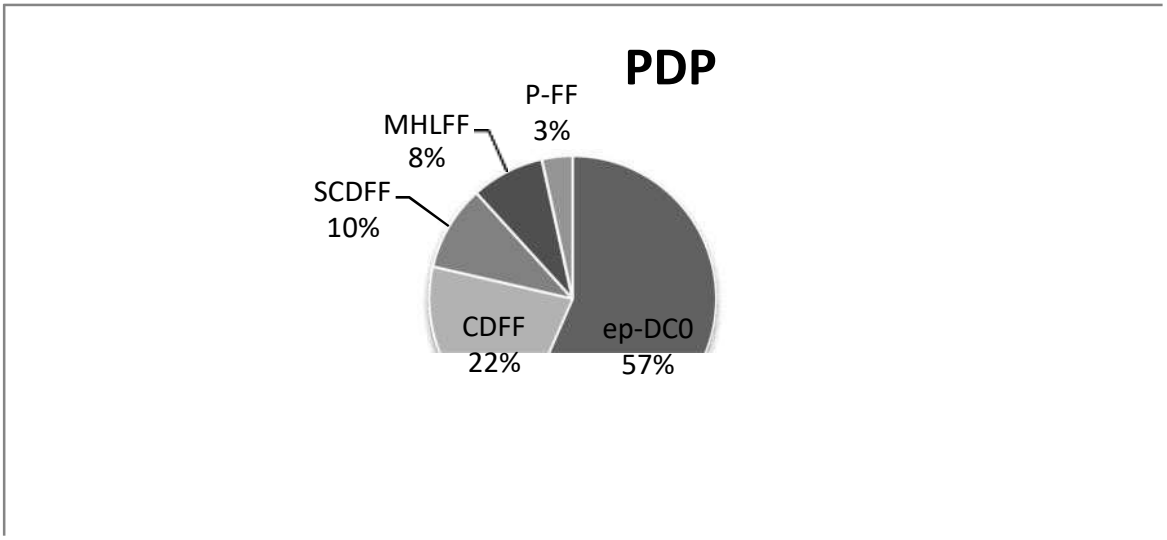
The performance of the proposed pulse trigger FF design is evaluated against existing designs through post layout simulations. The compared designs has include four explicit type P-FF designs shown in Fig. 1, A conventional CMOS NAND-logic-based pulse generator design with a three-stage inverter chain as show in Fig. 1(a)] is used for all pulse trigger FF designs except the MHLFF design, which employs its own pulse generation (PG) circuitry as specified in Fig 2.1(d)

The proposed target technology is the TSMC 90-nm CMOS process. Since pulse width design is important to the correctness of data capture and the power consumption, are sized for a design spec of 120 ps in pulse width in the TT case. The size of flip flop also ensures that the pulse generators can function properly in all process. With regard to the latch structures, each pulse trigger FF design is individually optimized subject to the product of power and D-to-Q delay i.e., input to output. To mimic the signal rise and fall time delays, input signals are generated with the help of buffers. Since the proposed design requires direct output driving from the input source, for comparisons the power consumption of the data input buffer (an inverter) has included. The output of

the flip flop is loaded with a 20-fF capacitor. Six test patterns and each representing a different data switching probability, is applied in simulations. Five of them are deterministic patterns, with 0% (all-0 or all-1), 12.5%, 25%, 50%, and 100% data transition probabilities respectively.

Table 1. Comparison of various P-FF designs

Explicit Flip flops	Avg.power (100%activity) µW	Avg.power (50% activity) µW	Avg.power (25% activity) µW	Data to Q Delay ps	Optimal PDP(50% activity) fJ
ep-DCO	17.4	14.6	14.5	128.83	1.88
MHLFF	17.9	15.5	14.6	156.30	2.42
SCDFF	17.3	14.7	13.7	120.89	1.77
CDFF	16.8	14.5	13.9	121.32	1.75
Proposed PFF	**14.5**	**12.7**	**12.9**	**111.67**	**1.41**



Graph 3.4 PDP of Explicit flip flops.

V. CONCLUSION

In this Paper, the various Flip flop design like, ep-DCO, CDFF, MHLLF, SCDFF, ,TSPC based P-FF & Proposed NEW P-FF are discussed. The pulse triggered Flip Flop (P-FF) design by employing two new design measures. The first one successfully reduces the requirement of number of transistors stacked along the discharging path by incorporating a PTL based AND logic. The second one has supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. These were been also designed in Hspice & Cosmoscop Tool those result waveforms are also discussed. This comparison table also added to verify the designed methods using CMOS 90-nm technology. With these all results Proposed P-FF performed speed or power better than EP-DCO, MHLLF, SCDFF and CDFF designs.

In this brief, we have presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design significant style consisting of a pass transistor and a p-seudo-nMOS logic. The key idea has been to provide a signal feed scheme through from input source to the internal node of the latch, which would be facilitate extra driving to shorten the transition time and enhance both power and speed performance of flip flop. The design was intelligently achieved by employing a simple pass transistor (MNx). Extensive simulations have conducted, and the results did support the claims of the proposed design in various performance aspects.

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