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Review of low-power double-tail comparator using different design

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ABSTRACT

The need for low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In order to achieve high-speed of comparator, to compensate the reduction of the supply voltages the larger transistors are required, which also means that more die area and power is needed. On the basis of the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double-tail comparator is modified for low-power and fast operation even in small supply voltages. The double-tail topology can operate faster and can be used in lower supply voltages, while consuming nearly the same power as the conventional dynamic comparator. Since, designing of double-tail comparator will give the better performance and optimized the power performance according to the CMOS technology used and the circuit operates on high-speed. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters (ADCs), as well as relaxation oscillators.

Index Terms— Double-tail comparator, high-speed analog-to-digital converters (ADCs), low power analog design.

I. INTRODUCTION

Comparator is one of the basic and important building-block in most of the analog-to-digital converter circuits (ADCs). Comparator is a device that compares two analog input voltages or currents and delivers a logical value at the output which indicates the polarity of input voltage difference. Designing high speed comparator is more challenging when the supply voltage is smaller. Due to fast speed, low power consumption, high input impedance and full-swing output, dynamic conventional comparators are very attractive for many applications such as high-speed ADC, memory sense amplifiers and data receivers.

A low-offset, low-power consumption, small area comparator is a very important circuit block for many applications, such as memory sensing circuits, analog to digital converters.(ADC), and so on. Therefore, offset voltage cancellation or calibration techniques are vital for realizing a low offset voltage comparator. In conventional designs, preamplifiers were used for offset voltage cancellation [2]. However, it increases power consumption because wide bandwidth amplifiers are required to reduce the offset voltage in the high frequency. A dynamic latched comparator shows higher load drivability than the conventional dynamic latched comparator. The addition of two inverters between the input and output stage of the conventional double-tail dynamic comparator, the regenerative latch stage was improved. Clocked regenerative comparators are fundamental circuit blocks, which are mostly based on cross-coupled inverters (latch) to force a fast decision due to positive feedback.

This type of comparator is typically used in Flash analog-digital converters (ADCs) because of their high decision speed. After designing the dynamic comparator, double-tail comparator is presented on this basis by adding few minimum-size transistors to the conventional dynamic comparator low-power and fast operation even in small supply voltages.

A clocked comparator is a circuit element that makes decision as to whether the input signal is high or low at every clock cycle. It has found widespread use in applications such as analog-to-digital (A/D) converters, wireline receivers, and memory bit-line detectors. To ensure correct detection on each comparison, the analog input must have sufficient magnitude to overcome deterministic errors such as offset and hysteresis, as well as random errors due to device thermal noise and flicker noise. Most comparators are triggered by periodic clocks and therefore can be treated as linear, periodically time-varying (LPTV) systems, which mend themselves well to the periodic simulation framework of RF circuit simulators including Spectra RF and ADS.

The pipelined ADC architecture has been adopted into many high-speed applications including high-performance digital communication systems and high-quality video systems [4], [14].

Another solution to this low op-amp gain problem is the use of correlated double sampling (CDS) technique [15]. CDS techniques have been used successfully in integrator and amplifier designs. With CDS, the

error resulting from the finite op-amp gain becomes inversely proportional to the square of the op-amp gain.

Comparators have a crucial influence on the overall performance in high-speed analog-to-digital converters (ADCs) [4]. Since, they are decision-making circuits that interface both analog and digital signals, which is often determined by its input-referred offset voltage, is essential for the resolution of high-performance ADCs[14].Dynamic double-tail comparators are widely used in high-speed ADCs due to its low power consumption and fast speed.

II. LITERATURE REVIEW

Reza Lotfi et.al gives a compressive delay analysis of the dynamic comparator for various architectures. The conventional dynamic comparator is mostly used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power Consumption. In the given technology, Additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. Due to the better performance of conventional dynamic comparator in low voltage application, conventional dynamic double-tail comparator is designed on the basis of conventional dynamic comparator which operates on low-power and low supply voltages. The given circuitry has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. [1]

Masaya Miyahara et.al developed low-offset latch comparator by using new offset cancellation technique. The developed comparator requires two phase such as reset mode and regeneration mode. The offset voltage of the comparator is caused by the mismatch of the transistor's threshold voltages. Therefore, due to input common mode variation increasing offset voltage can be suppressed by using the given methodology. The offset voltage cancellation or calibration techniques are vital for realizing a low voltage offset comparator. Conventional double-tail latched comparator had been designed by using conventional latched comparator. Each stage's contribution to the offset voltage of the conventional comparator obtained from Monte-Carlo simulation. Dynamic offset cancellation techniques that require no static current were developed for lathed comparator. [2]

Jaeha Kim et.al describes a framework based on linear time-varying system theories that can accurately analyze and simulate the random decision error probabilities in clocked comparators. Author presents the analysis and simulation methodologies for characterizing the random decision error probabilities in clock comparators based on an LPTV system model. However, practical comparator circuits do not have such explicit distinction between these filtering, sampling, and decision operations is applicable for understanding the design trade-offs in clocked comparators as well as estimating their random decision error probability using the RF simulation techniques, this mathematical model is useful for analyzing the comparator characteristics and quantifying the decision error probabilities. For the purpose of estimating the random decision error, or equivalently the input-referred noise, author primarily interested in the LTV system response of the comparator in the sampling phase and in the regeneration phase. In many applications comparators are preceded by LTI circuits such as equalizers and pre- amplifiers which can add noise to input signal and contribute to the random decision error probability. [3]

Un-Ku Moon et.al implemented the technique which is highly effective for finite op-amp gain compensation in the context of low-voltage and high-speed pipelined ADCs. This technique enables low-power and high-speed operation by allowing significantly reduced amplifier gain. Another solution to solve this low op-amp gain problem is the use of correlated double sampling (CDS) technique. CDS techniques have been used in the design of integrator and amplifier. The most important goals of the time-shifted CDS techniques are to eliminate the one extra clock phase and to realize the pre-sampling and real sampling in different clock phases to avoid added capacitive loading. No offset cancellation scheme is employed because large comparator offsets can be tolerated in pipelined ADCs. The finite op-amp gain is becoming a major hurdle in achieving both high speed and high accuracy. [4].

Sanyi khan et.al developed the technology to analyze the static input offset voltage in a dynamic comparator in the same way as in the traditional operational amplifier. However, in dynamic comparators with an internal positive feedback, the previous method is not applicable. The authors fail to clearly the state how to determine the value of transconductance and output conductance of the transistors at time-varying condition. In this method, we first solve the bias point at comparison phase when the circuit is perfectly balanced without any mismatch. Second, very little emphasis is placed on mismatch of internal parasitic capacitance. [5]

III. UDSM CMOS TECHNOLOGY

The comparator circuit was designed using general 180 nm CMOS process. The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1 [1], [6]. The comparator operates in two phases is as follows. During the reset phase when CLK = 0 and Mtail is off, reset transistors (M7–M8) pull both output

nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5).

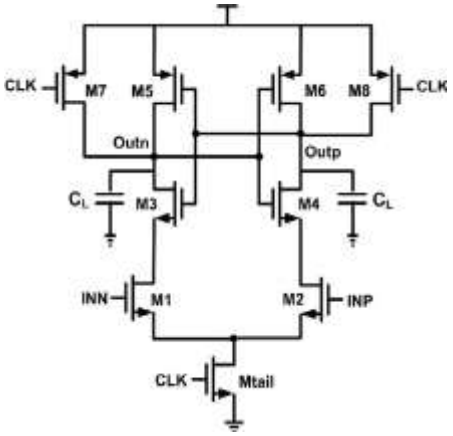

Fig.1- Schematic diagram of the conventional Dynamic Comparator [1]

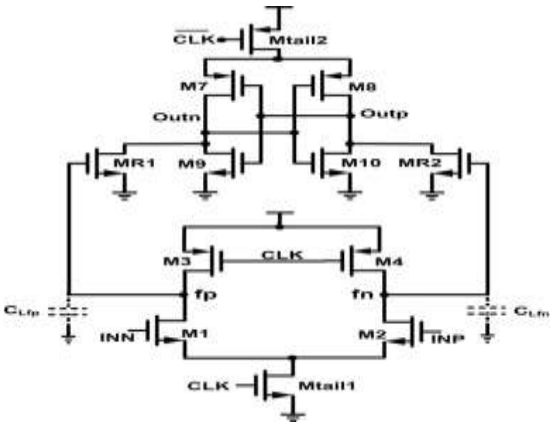

Fig.2-Schematic diagram of conventional dynamic double-tail comparator [1]

A conventional double-tail comparator is shown in Fig. 2 [10]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset [10]. This comparator operates in two phases as follows. During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an input-dependent differential voltage _Vfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes _Vfn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [10].

The delay of this comparator comprises two main parts, t0 and tlatch. The delay t0 represents the capacitive Charging of the load capacitance CLout (at the latch stage output nodes, Outn and Outp) until the first n-channel transistor (M9/M10) turns on.

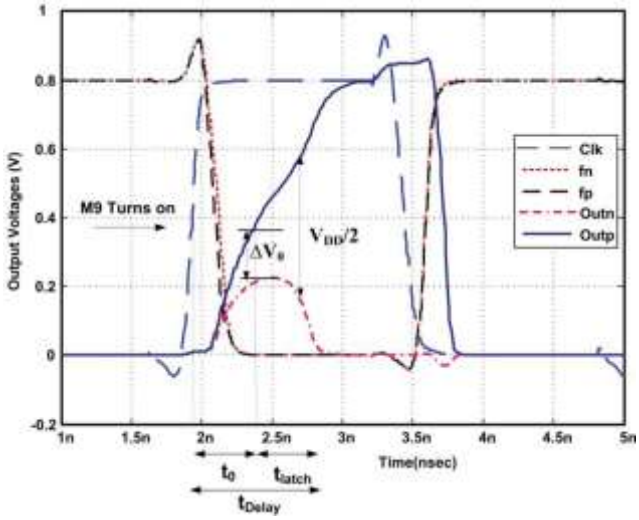

Fig.3-delay analysis [1]

IV. OFFSET VOLTAGE CANCELLATION TECHNIQUE

The offset voltage of the comparator is caused by the mismatch of the transistor's threshold voltages. Figure 4 shows the conventional double-tail latched comparator circuit [2] and signal behaviour. Moreover, each stage's contribution to the offset voltage of the conventional comparator obtained from Monte-Carlo simulation is shown in Fig. 4. The comparator circuit was designed using general 90 nm CMOS process.

The offset voltage of the 2nd stage is relaxed by conversion gain *G*1 between the 1st stage and 2nd stage. On this account, mismatch of the 1st stage transistors becomes dominant in the comparator offset voltage. Furthermore, most of the offset voltage of the 1st stage is caused by the mismatch of the input transistor's (M1, M2) threshold voltages. Therefore, the offset voltage of the comparator can be suppressed by cancelling the threshold voltage mismatch of the input transistors.

In case the mismatch threshold voltage M1 and M2 can be cancelled, the offset voltage of the 2nd stage becomes dominant in the comparator offset voltage. G1 must be kept high to reduce the 2nd stage offset voltage. However, G1 is affected by the input common mode voltage Vcm_i variation. For instance, the offset voltage increases from 1.35 mV to 8.7 mV at 1 sigma when Vcm_i changes from 0.4 V to 0.9 V. This means that G1 is decreased to 1/6 by changing the input common mode voltage. When the input common mode voltage is determined by the output common mode voltage of the preamplifier, the offset voltage will increase. Therefore, the circuitry that can decide *G*1 without being affected by the input common mode voltage of the comparator should be developed.

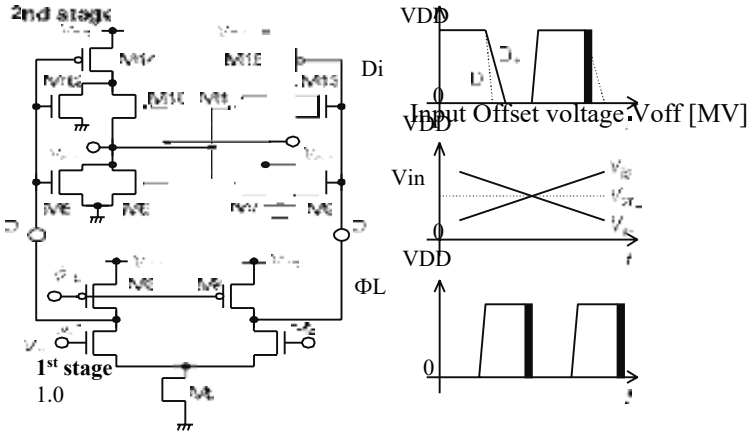

Fig.4-The conventional double tail latch comparator [2]

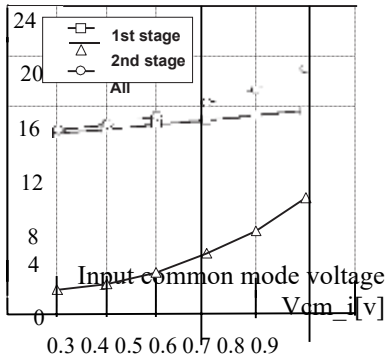

Fig.5-Each stage's contribution to the offset Voltage [2]

V. LINEAR TIME VARYING TECHNIQUE

The clocked comparator model basically consists of three main elements: a noisy nonlinear filter, an ideal sampler, and an ideal slicer. On the basis of this model, the probability of a decision error can be determined by the signal-to-noise ratio (SNR) at the slicer input. While practical comparator circuits do not have such explicit distinction between these filtering, sampling, and decision elements.

The LTV filter model also includes an additive Gaussian noise process at the output of the filter. While in general the noise is a time-varying noise process, for the purpose of estimating decision error probabilities, they only interested in the variance in at a specific time point, the sampling instant of the internal model sampler. This noise variance can be derived using either (3) or (11) depending on the type of the input noise source.

. As previously mentioned, they treat a clocked comparator as a LTV system whose linear system response changes over time. In case of the comparator circuit, the comparator goes through a set of distinct operating phases each cycle, namely: resetting, sampling, regeneration, and decision phases.

For the purpose of estimating the random decision error, or equivalently the input-referred noise, they are primarily interested in the LTV system response of the comparator in the sampling phase and in the regeneration phase. Within each phase, the small-signal circuit parameters such as transconductance would stay constant. Practical comparator circuits do not abruptly transition from one phase to another; rather their characteristics change continuously with time. However, this approximation serves well the purpose of identifying the key design tradeoffs governing the input-referred noise of the comparator.

Initially, the comparator is in the resetting phase when the clock input clk is low. The reset switches M4 and M4' pull the output nodes +output and -output to Vdd and the internal nodes X and X' to Vdd-VTn approximately, where VTn is the threshold voltage of an nMOS transistor. During this phase, the noise currents from the reset switches can contribute to the noise voltages on the output nodes.

When clk switches to high at t=t0, the input differential Pair M1 and M1' starts discharging the nodes X and X' depending on the input voltage difference. The cross-coupled nMOS pair M2, and M2' then discharges the output nodes i.e. +output and -output depending on the voltage difference between X and X'. Hence, the comparator is sampling the input voltages onto the internal nodes X/X' and the output nodes Out+/Out-. Until the voltage on +out or -out drops below Vdd-VTp, where VTp is the threshold voltage of pMOS, the pMOS cross-coupled pair M3 and M3' remains in cut-off state. Let's assume this sampling phase lasts until.

The approximate small-signal model for the comparator is found in the sampling phase. The drain current noise sources in1 and in2 are shown from the transistors M1 and M2 respectively. From this small-signal model, they can derive the transfer function from the small-signal input Vin to the small signal output Vout as the following:

$$Vout(s)/Vin(s) = gm1.gm2/S.Cout.Cx(s+gm2\ (Cout-Cz/Cout.Cz))$$

Where gm1 and gm2 are the transconductances of M1 and M2, respectively, and Cx and Cout are the total capacitances associated with the nodes X and out, respectively.

In the regeneration phase, When the output nodes out+ and out- fall sufficiently low that the pMOS devices M3 and M3' finally turn on, the cross coupled inverter pair M2-M2'-M3-M3' starts regenerating the voltage difference stored on the output nodes via positive feedback. During this phase, we assume that the input devices M1 and M1' are in linear region with very large conductance compared to the other devices; hence the internal nodes X and X' are considered almost short-circuited to ground as in [12].

The small-signal model of comparator in also implies that the comparator is no longer sensitive to the input voltage and also to the noise current from the input devices M1 and M1' once the regeneration starts.

VI. TIME-SHIFTED CDS TECHNIQUE

The most commonly used capacitively coupled comparator is adopted in sub-ADC design as shown in fig. since, the input capacitance is 0.1uf. No offset cancellation scheme is employed because large comparator offsets can be tolerated in 1.5-b/stage pipelined ADCs. The time-shifted CDS technique does make this tolerance smaller. One critical part of this comparator module is the latched comparator, which is shown in fig. It includes three stages: input amplifier (M1 and M2), NMOS and PMOS regeneration latches (M5–M8), and output S-R latch (M13–M20). The input amplifier is a simple NMOS differential pair with 300- A bias current, which not only amplifies the input signal but also suppresses the kickback noise from the regeneration latches. The NMOS switches (M3 and M4) will turn off the input differential pair during regeneration time in order to save power consumption. It also helps reduce kickback noise from the regeneration latches. The combination of PMOS and NMOS regeneration latches speeds up the regeneration compared to the PMOS-only latches. The regeneration latches are reset to a voltage close to power supply by M11 and M12 during the sampling/resetting phase. One additional reset switch, M10, across the differential latching node reduces the offset due to the mismatch of M11 and M12. The NMOS switch M9 disables the NMOS regeneration latch during the resetting phase to avoid large dc current to ground. The output S-R latch holds the comparison result during the whole clock period for the convenience of following encoding logic. With about 0.3 mW at 1.8 V, this latched comparator achieves less than 250-ps regeneration time for a 2-mV differential input signal, which is short enough for a 100-MHz clock with 400-ps non-overlap time.

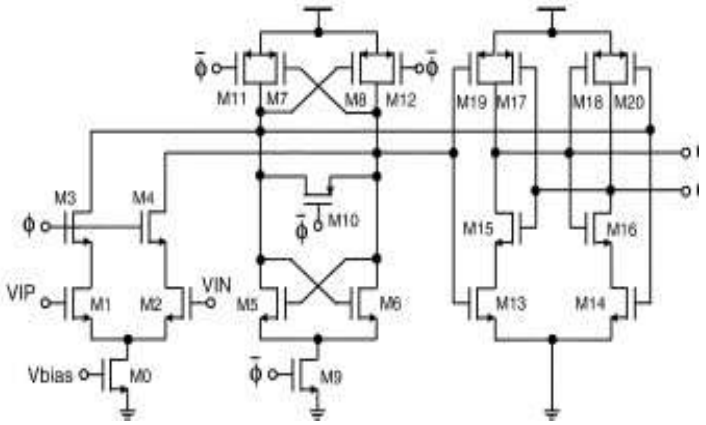

Fig.6- Latched comparator [4]

VII. NOVEL BALANCED METHOD

A fully differential dynamic comparator will maintain a balanced state if no mismatch exists in the circuit. The comparator circuit was designed using general 0.25 um CMOS process. For static offset voltage, balanced state means that Vout+=Vout-; currents I1 and I2 in both branches are identical at all times during the transient process. The balanced state can be described by a space φb comprised of power supplies, external bias voltage Vlatch and comparison threshold or reference voltages Vref+ and Vref- and transistor node voltages, which is written as φb = {Vdd, Vlatch, Vref+, Vref-, Vs5 or Vs6, Vd5 or Vd6, Vout + or Vout-}, in which the subscripts and mean source and drain voltage of transistor, respectively. When mismatch occurs, the circuit will lose its balance so that Vout+ is not equal to Vout-. A voltage ΔVin can be applied to compensate the mismatch effect and make Vout+ equal to Vout- . This compensation voltage ΔVin is the input offset voltage. The new balanced state Φbn is the same as Φb, because mismatches are small disturbances that will not change the bias condition of the comparator.

When the control signal Vlatch reaches VDD is chosen. Therefore, the operation regions of all of the transistors are well defined. Transistors of M1-M4 connecting to the input and reference voltages are in the triode region and act like voltage-controlled resistors. M10 and M11 have equal drain and gate voltage, which makes them work at saturation region. M7and M8 work as switches embedded in cross-coupled inverter pairs made of M5-M10 and M6-M11. They are turned on during comparison phase and working in the triode region because of its high gate voltage Vg7, 8=VDD. The drain voltage of M5 and M6 is pulled up closed to Vout+ or Vout- and works in saturation region. M9 and M12 are both turned off because control signal Vlatch is VDD, which indicates that mismatch effects in M9 and M12 are negligible. Once the operation region for each transistor is known, combining with known power supply voltages, input voltages and process parameters, each node voltage in the dynamic comparator at balanced state can be readily solved.

If other time point for the analysis is chosen, for instance, when Vlatch is half of the VDD, the operation regions of M7 and M8 becomes unclear. In that situation, the operation regions need to be assumed first, and then verified by solving each node voltages under the balanced condition. Iteration may be necessary to find the operation region of M7 and M8.

The analytical model also gives a good prediction to the offset in the second topology dynamic comparator. A good agreement between the simulated values and derived values shows the effectiveness of this balanced method. The derived analytical expressions provide deeper insights in the most dominant offset contributors and design tradeoffs. This method is reliable and more efficient.

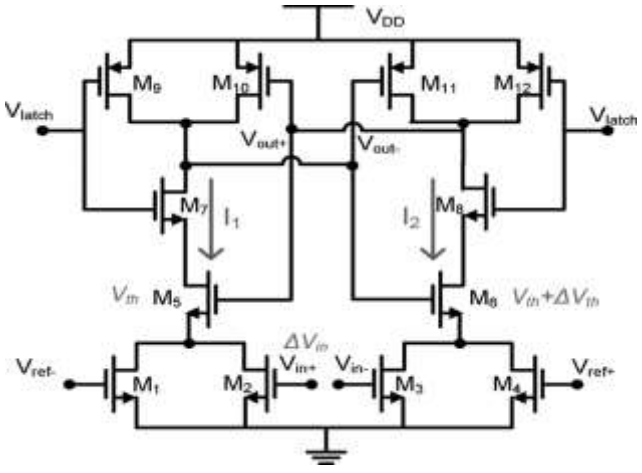

Fig.7-Lewis-Gray Structure [5]

VIII. COMPARISON TABLE TABLE 1

Method	Technology CMOS	Supply Voltage	Max. Sampling Frequency	Power Consumption	Estimated Area
1]	180nm	0.2v	900MHz	128uw	16u*16u

2]	90nm	1.2v	500MHz	39uw	152um^2
3]	90nm	1.2v	1.6 GHz	-	150um^2
4]	0.18um	1.8v	100MHz	67mw	1.2mm*1.2mm
5]	0.25um	1.5v	10MHz	74mw	1.5u/0.45u

IX. DESIGNING OF LOW-POWER ADC USING DOUBLE-TAIL COMPARATOR

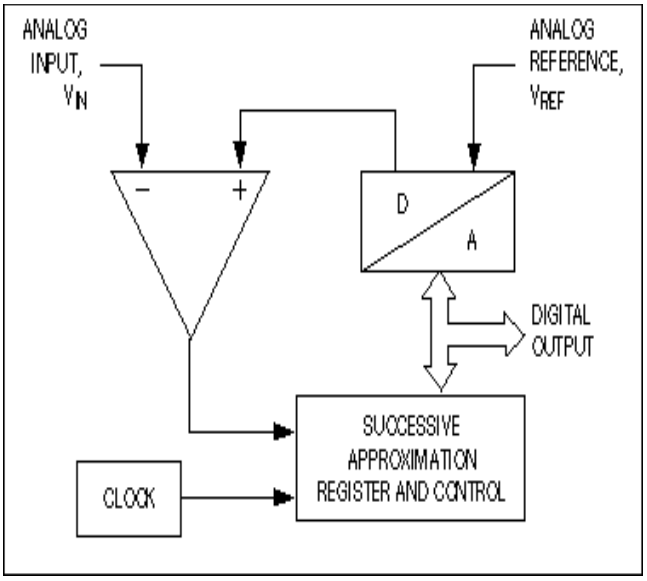

Fig.8-Block diagram of ADC using double-tail comparator

For the designing of many high-speed ADC, high-speed, low voltage, low-power double-tail comparator with small chip area is required. In order to achieve the to achieve high speed of the given comparator, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Since, by using this low-power double-tail comparator the designing of low-power ADC is very easy which also gives better performance and operate with high-speed.

X. CONCLUSION

The designing of low-power double-tail comparator using the above methods suggest that UDSM CMOS technology is more reliable for the estimation and optimization of power performance. A new Dynamic double-tail comparator with low-voltage, low-power capability is developed in order to improve the performance of the comparator. UDSM CMOS technology has better performance and speed. Double-tail structure takes advantage of input-output isolation and minimum kickback noise, similarly also keeps the advantage of speed enhancement and power reduction.

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