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High Speed and Low Power FIR Filter Implementation Using Optimized Adder And Multiplier Based On Xilinx FPGA

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ABSTRACT

Finite impulse response (FIR) filters are widely used in various DSP applications. The low-power or high speed techniques developed specifically for digital filters can be found in. Many applications in digital communication, speech processing (adaptive noise cancelation), seismic signal processing (noise elimination), and many other synthesis operations of signal require large order FIR filters ,since the number of multiply-accumulate (MAC) operations required per filter output increases linearly with the filter order, hence implementation of these filters of large orders is a challenging task. Here, we propose designing of FIR filter using high speed low-power multiplier adopting the new implementing approach. The multiplier we are using is Vedic Multiplier. It will reduce the number of partial products generated by a factor of 2. The carry save adder will avoid the unwanted addition and thus minimize the switching power dissipation. The architecture is designed in VHDL, simulate and synthesize in Modelsim and Xlinx ISE Software .
Index Terms: FIR, VHDL, Xilinx ISE.

I. INTRODUCTION

Finite impulse response (FIR) filters are highly used in most of the DSP applications. In most of the applications, the FIR filter circuit must be able to operate at high sampling rates, while in many applications, the FIR filter circuit must be a circuit operating at moderate sample rates and uses low power. Parallel processing techniques can be applied to digital FIR filters to either increase the effective speed or reduce the power consumption of the original filter. Not much of work has been done that dealing with reducing the hardware complexity or power consumption of parallel FIR filters. From many years parallel processing applied to an FIR filter involves the hardware units replication that exist in the original filter. The choice of the multiplier circuit also affects the resultant power consumption. If the multiplier is choosen wisely with less number of calculations, both speed and power can be optimized.

Multipliers play an important part in digital signal processing systems. Multipliers consume considerable power have large area and long latency. Therefore, multiplier with low power design has been an important part in low-power VLSI system design. The main research of this work is optimization of multiplier designs produces more power-efficient solutions than optimization only at low levels. Specifically, we consider how to optimize the internal algorithm and architecture of multipliers and how to control active multiplier resource to fullfil the need. The main objective is reduction in power with small area and delay. Using new architectures or algorithms, it is possible to optimize power, speed and area.

FIR FILTER THEORY

Digital filters are typically used to modify or alter the characteristics of a signal in the time or frequency plane. The digital filter mostly used is the linear time-invariant (LTI) filter. An LTI communicates with its input signal through a process called linear convolution, denoted by y = f _ x where f is the impulse response of filter, x is the applied input signal, and y is the convolved output. The convolution process (linear) is formally defined by:

y[n] = x[n] * f[n] =□ x[n]f[n-k]=□ f[k]x[n-k]. (1) k=0

LTI digital filters are generally classified as being finite impulse response (i.e., FIR), or infinite impulse response (i.e., IIR). As the name implies, an FIR filter consists of a finite number of samples , reducing the convolution sum to a finite sum per output sample instant. An FIR filter having constant coefficients is an LTI digital filter. The FIR filter's output of order L, to an input time series x[n], is given by a finite version of the convolution sum given in (1), namely:

L-1

y[n]=x[n]*f[n]=□ f[k]x[n-k], (2) k=0

Where f[0] □ 0 through f[L □ 1] □ 0 are the filter's L Coefficients. They also correspond to the FIR's impulse

response. For LTI systems expressed in the z-domain with Y(z)=F(z)X(z), (3)
Where F(z) is the transfer function of FIR filter defined in the z domain by L-1
F(z)= □ f[z]z-k (4) k=0
The Lth-order LTI FIR filter is graphically shown in Fig.1. It consist of a collection of adders, multipliers and tapped delay lines. One of the value presented to each multiplier is an FIR coefficient, often referred to as a "tap weight". The FIR filter can also be called as "transversal filter," suggesting its "tapped delay line" structure.

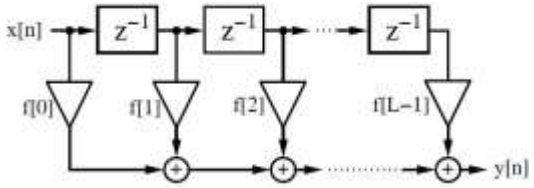

Fig. 1: FIR filters in the transposed structure.

CARRY LOOK AHEAD ADDER

A carry-look ahead adder (CLA) is a type of adder used in digital system. A carry-look ahead adder improves speed by reducing the amount of time required to wait for the carry bits. It can be compared with the simpler, but usually slow, ripple carry adder for which the carry bit is calculated side by side with the sum bit, and each bit waits till the previous carry has been calculated to begin calculating carry bits and its own result. The CLA adder calculates one or more carry bits before doing the actual sum, which minimizes the wait time to calculate the result of the larger value bits.

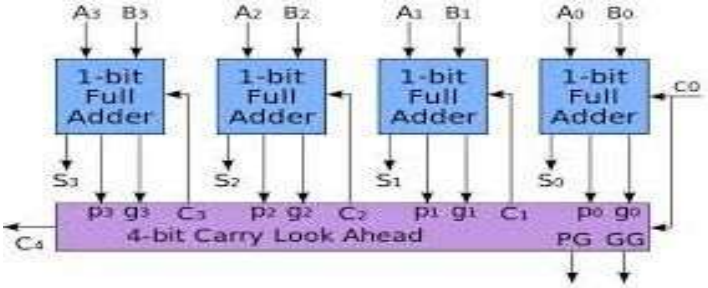

Fig. 2: 4-bit Carry Look Ahead Adder

Let ai and bi be the augends and addend inputs, ci the carry input, si and ci+1 , the sum and carry-out to the ith bit location. The pi and gi (auxillary functions) are called the propagate and generate signals, the output of adder is given by:
pi = ai + bi gi = ai bi
si = ai xor bi xor ci ci+1 = gi + pici

VEDIC MULTIPLIER

The multiplier architecture is based on this Urdhva tiryakbhyam sutra. The benefit of this algorithm is that partial products and their sums are calculated simultaneously. This makes the multiplier clock independent. Regularity is the another advantage of this multiplier as compared to many other multipliers. Hence lay out design will be easy due to its modular nature. The architecture can be ellaborated using two 8 bit numbers i.e. the multiplier and multiplicand are 8 bit numbers. The multiplicand and the multiplier bits are divided into four bit blocks. These four bit blocks are again splitted into two bit multiplier blocks. According to the algorithm the 8 x 8 (A x B) bit multiplication will be as follows.

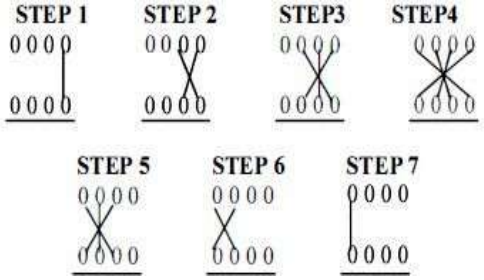

Fig. 3: 4*4 Multiplication technique using Urdhva tiryakbhyam sutra.
A=A7A6A5A4A3A2A1A0 B=B7B6B5B4B3B2B1B0
AH=A7A6A5A4,AL=A3A2A1A0BH=B7B6B5B4,BL=B3B2B1B0 By using algorithm, the product obtained is as

follows.

Product of A x B = AL x BL + AH x BL + AL x BH+AHxBH

II. THE PROPOSED ARCHITECTURE

An approach to the implementation of digital filter algorithms based on field programmable gate arrays (FPGAs) was described. General purpose DSP implementations often lack the performance necessary for moderate sampling rates, and ASIC approaches are limited in flexibility and may not be cost effective for many applications. Because of the programmability of this technology, the examples in the paper can be extended to provide a variety of other high performance FIR and IIR filter realizations [7]. Then multiplierless technique was presented, based on the add and shift method and common subexpression elimination for low area, high speed and low power implementations of FIR filters. They validated their techniques on Virtex IITM devices where they observed significant area and power reductions over traditional Distributed Arithmetic based techniques [6]. Then a clear concept of different multiplier and their implementation in tap delay FIR filter was obtained. They found that the parallel multipliers are much option than the serial multiplier. They concluded this from the result of area and power consumption. In the case of parallel multipliers, the area is much less than that of serial multipliers. Hence the power required is also less. This fasten up the calculation and makes the system fast. After comparing the radix and the radix modified booth multipliers they found that radix consumes lesser power than that of radix. In the end it is determined that modified booths Algorithm work the best [4]. Then a novel design for a FIR filter using Parallel Multiplier with carry save adder (Modified Booth Algorithm was introduced. The implementation of the algorithm with an architecture and logic design is presented where in the Speed, Power and design are compared to other architectures. Again, the proposed design is an area efficient multiplier useful in decreasing area consequently reduces the cost. The delay encountered is reduced and the processing speed is increased than those obtained in other conventional techniques. The proposed activity evaluation method leads to consumed low power estimations and very fast estimation times [3]. Then four new architectures are presented, Mac Fir Filter Based Booth Multiplier, Linear- Phase-Folding Architecture Fir Filter Based Booth Multiplier, FIR Filter Based Shift/ Add Multiplier, Mac Fir Filter Based Low Power Serial Multiplier and Serial Adder and the delay of these architectures are respectively 5.20ns, 7.336ns, 9.181ns and 6.457ns respectively. Power of these architecture are 0.87mw, 0.90mw, 0.88mw and 0.86mw respectively [2]. Low power and low area FIR filter was designed and implemented. To reduce power consumption and area they used combination booth multiplier, low power serial adder and serial multiplier, multiplier base on shift/add in two forms and technique folding transformation in linear phase. These filters were compared for area and power with other common implementations and it demonstrated that this approach is most effective for implementations with the constraints of low cost and low power [1].

In our project, we analyze the different architecture of adders and multipliers. In our case we are going to consider Vedic multiplier for the operation of FIR Filter. Also, we are analyzing the area resource utilization, power and time delay for FIR filter architecture.

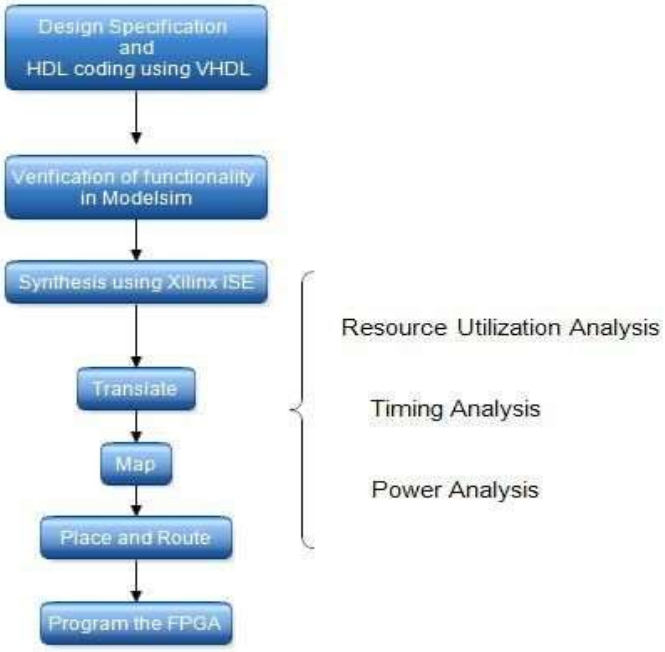

Fig. 4: Steps involved in Design & Implementation

III. SIMULATION AND RESULTS

In this work we are evaluating the performance of the proposed FIR filter using low power consumption multiplier by comparing vedic multiplier with the different multipliers. These multipliers can be implemented using VHDL coding. In order to get the power report and delay report we are synthesizing these multipliers using Xilinx and Modelsim. Simulation result for the FIR filter using Vedic multiplier are given in figure.

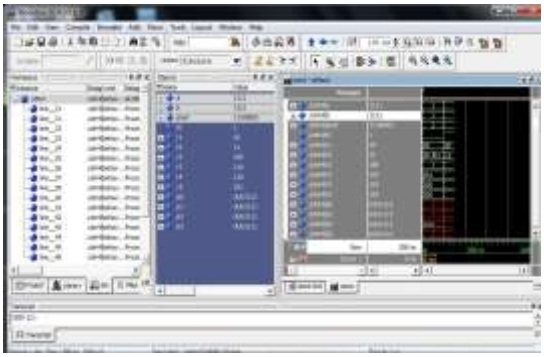

Fig. 5: Simulation Result for Vedic Multiplier

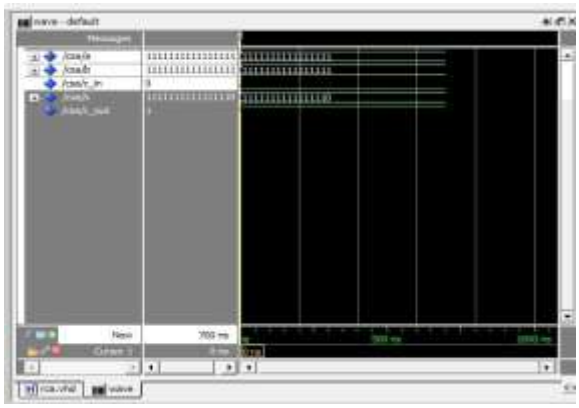

Fig. 6: Simulation Result of Carry Look Ahead Adder

IV. COMPARISIONS

Designs equipped to 8bit adders and 8bit multiplier and are achieved via VHDL hardware description language using Xilinx ISE software synthesized and implemented on FPGA in Virtex IV family. Also power is analized using Xilinx XPower analyzer. Table shows the comparison between powers
Consumption the type of device that has been used in different articles and the characteristic of our filters designed.

Table 1: Power Consumption For Different Mutipliers

Fre qn	Signe d array multi plier mw	Booth withou t DPDT mw	Booth with DRD	Booth with DPDT using REG mw	Booth with DPDT sing And gate
25	612	469	423	326	868
50	1170	879	851	596	669
75	1173	1297	1256	881	1018
100	2293	1703	1658	1137	1283

V. CONCLUSIONS

In this paper, we presented a low power, high speed and low area FIR filter. For reduce power consumption combination of vedic multiplier , low power serial multiplier and serial adder. Multipliers based on shift/add in two forms and technique. Folding transformation in linear phase . These filters were compared for power and speed with other common implementations and demonstrated that our approach is most effective for implementations with the constraints of low cost and low power. Our proposed FIR filters have been synthesized and implemented using Xilinx ISE Virtex IV FPGA and power is analysed using Xilinx X power analyzer.

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