



# ROLE OF VHDL IN DIGITAL SYSTEM DESIGN

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## ABSTRACT

*This paper describes the design and implementation of 4x1 MUX and ALU using VHDL. Results include successful compilation of VHDL code in Quartus II, waveforms show verification of truth table, the results are also verified in analog domain using analog simulation. It also shows layout level implementation of 4x1 MUX and ALU using Microwind tool, it also shows technological view of 4x1 MUX and ALU along with chip floor plan.*

**Keywords** –4x1 MUX, ALU, VHDL, Analog, Layout, Chip floor plan

## I. INTRODUCTION

The term digital system includes the various systems from low level components to complete systems over a chip and board-level design. Considering a digital system and its complexity, it is not possible to understand such a complex system completely, so to make design of a system less complex and understandable VHDL is used. This paper describes the implementation of 4x1 MUX and ALU using VHDL technology which meets less complexity requirements; it also shows how efficiently a digital system i.e. 4x1 MUX and ALU is implemented up to layout level. Results show technological map, RTL view, chip floor plan, chip layout, output waveforms showing voltage Vs time relations and verification of truth table.

## II. 4X1 MUX DESIGN

4x1 mux is a combinational circuit that has an ability to increase the amount of 4 bit data that can be sent over the network within a certain amount of time and bandwidth. A 4 bit input provides using 2 select lines and produces a proper output. Fig (1) shows logic diagram of 4x1 mux. Table (1) shows truth table of 4x1 mux. A multiplexer is also called a data selector. In analog circuit design, a multiplexer is a special type of analog switch that connects one signal selected from several inputs to a single output. In digital circuit design, the selector wires are of digital value.

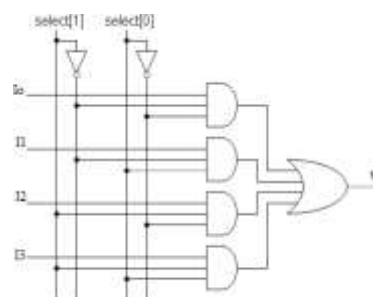


Fig.1 : Logic diagram of 4x1 MUX

$s_1$	$s_0$	$x_3$	$x_2$	$x_1$	$x_0$	$y$
0	0	x	x	x	0	0
0	0	x	x	x	1	1
0	1	x	x	0	x	0
0	1	x	x	1	x	1
1	0	x	0	x	x	0
1	0	x	1	x	x	1
1	1	0	x	x	x	0
1	1	1	x	x	x	1

Table 1 : Truth table of 4x1 MUX

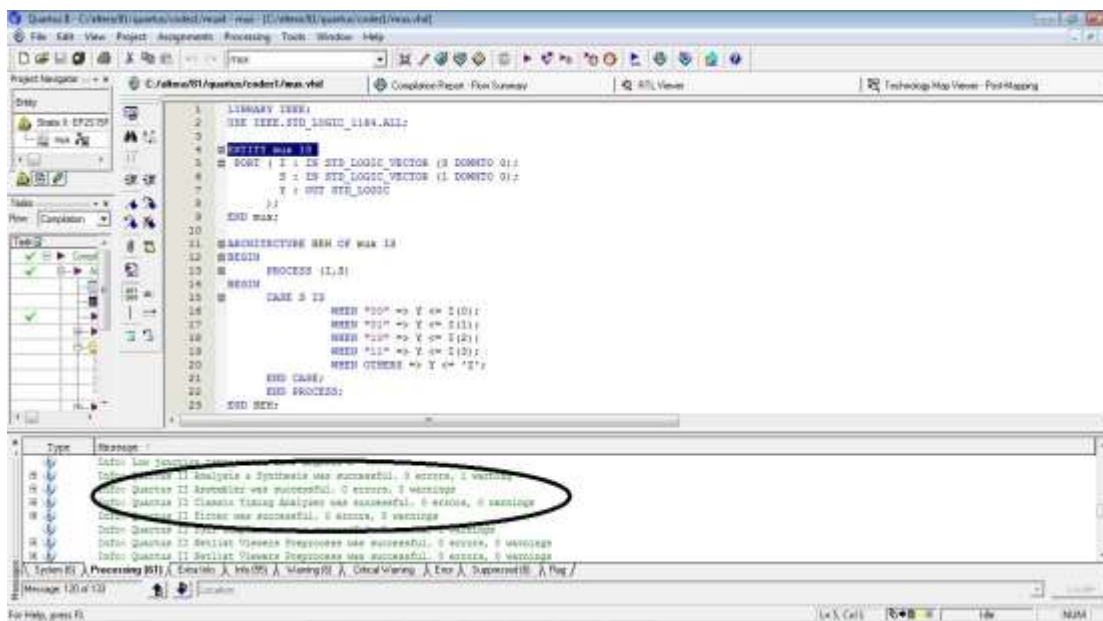
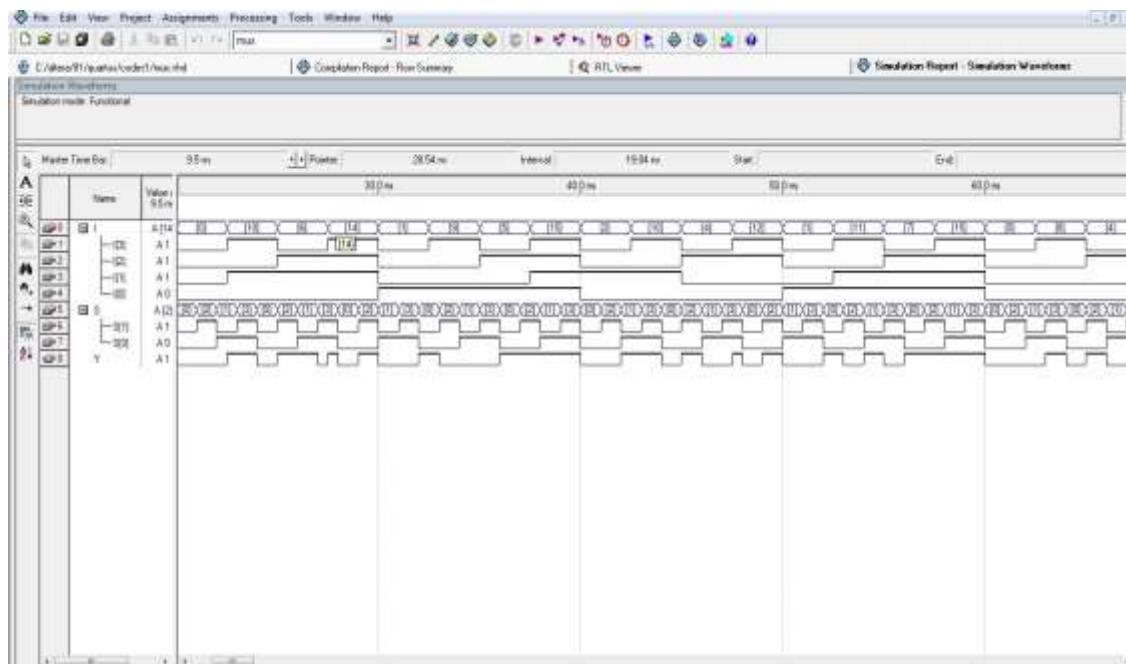


Fig 2.1: VHDL Code compilation



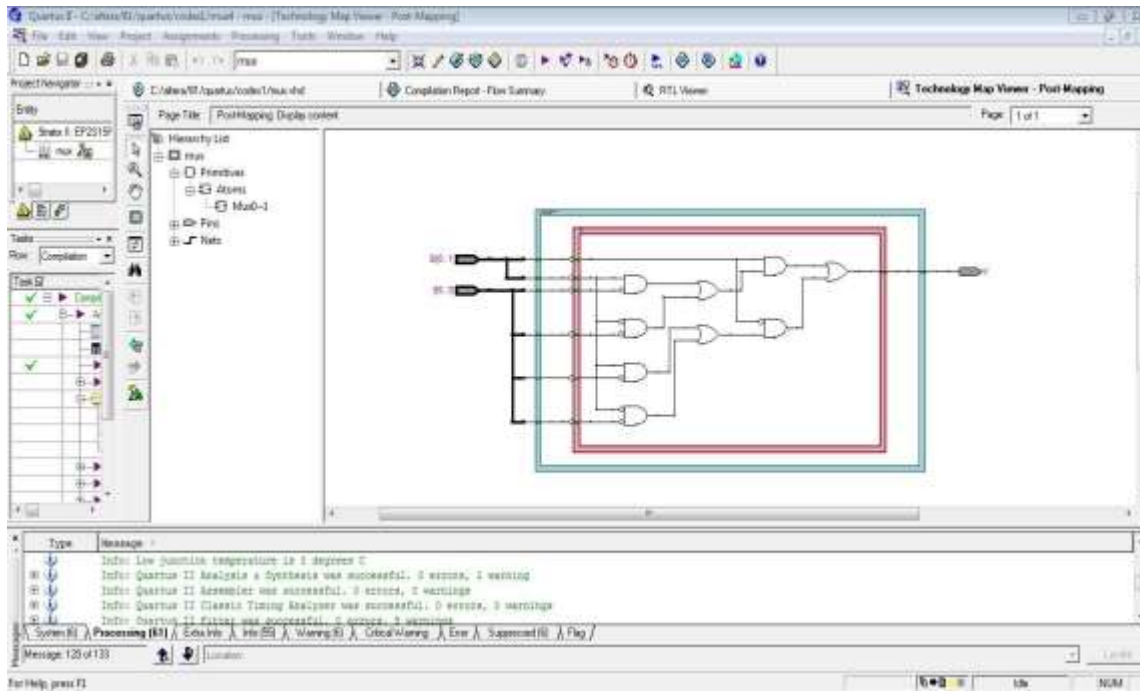


Fig 2.3: Technological map view

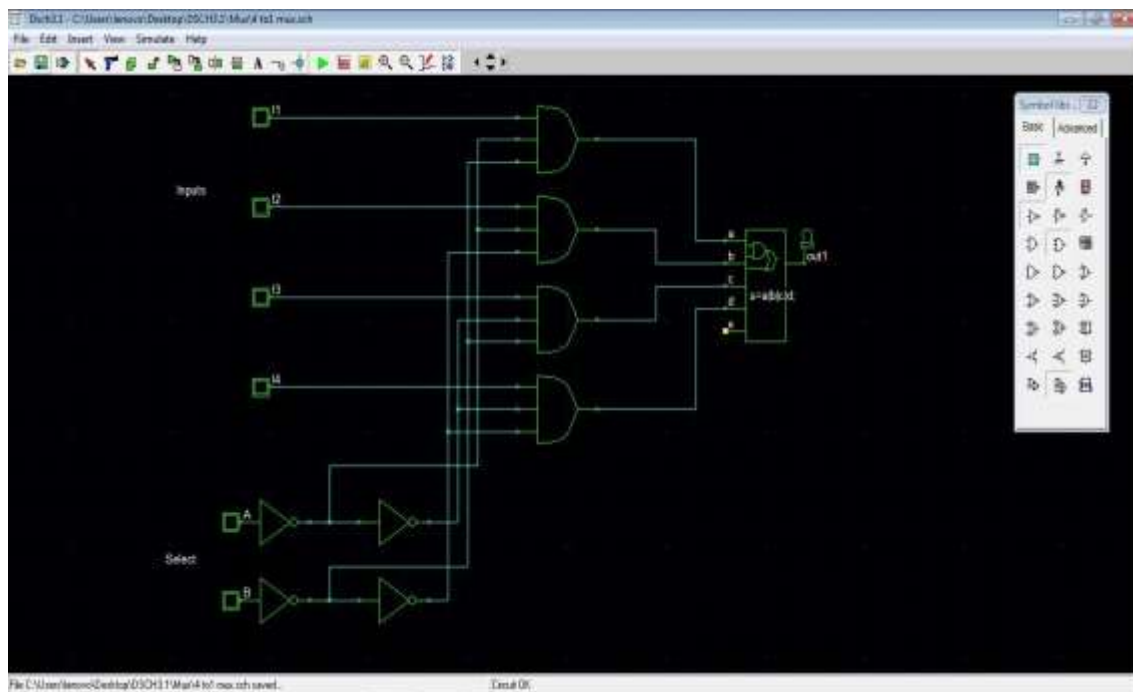


Fig2. 4: Schematic of 4x1 MUX before execution in analog domain

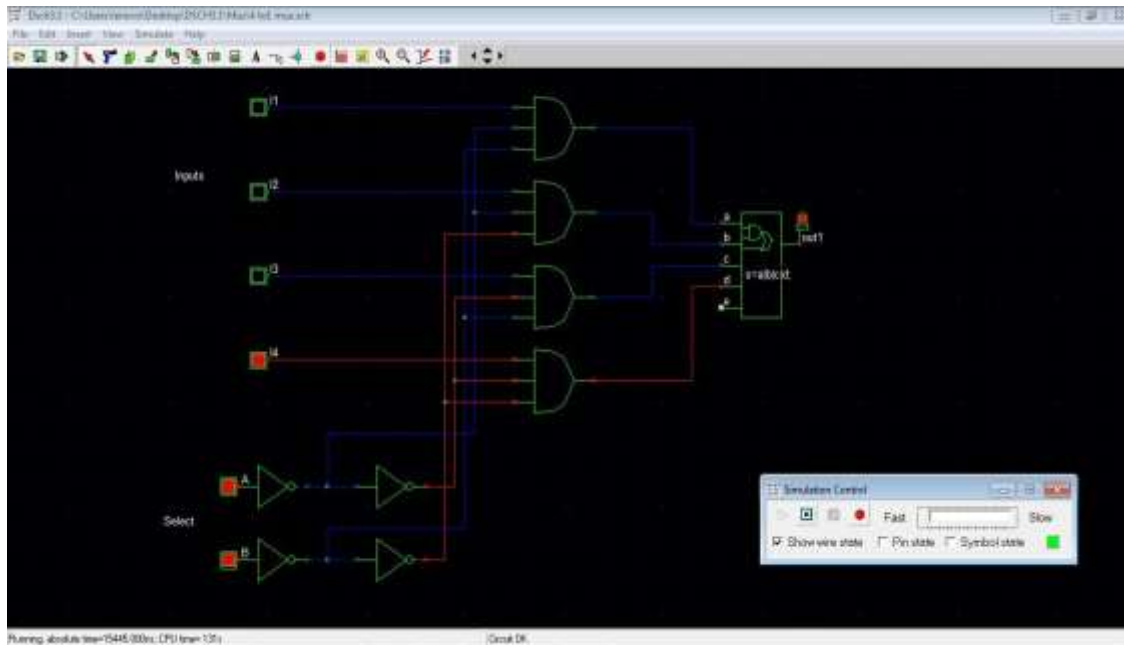


Fig 2.5: Schematic of 4x1 MUX after execution in analog domain

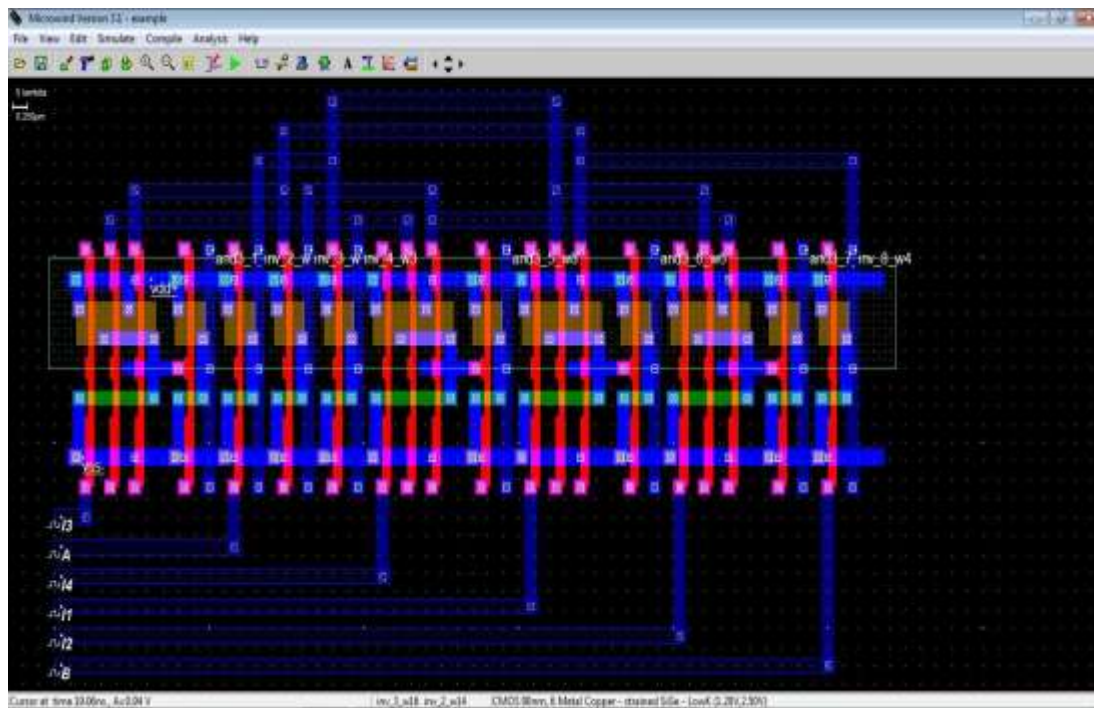


Fig 2.6: Layout of 4x1 MUX circuit

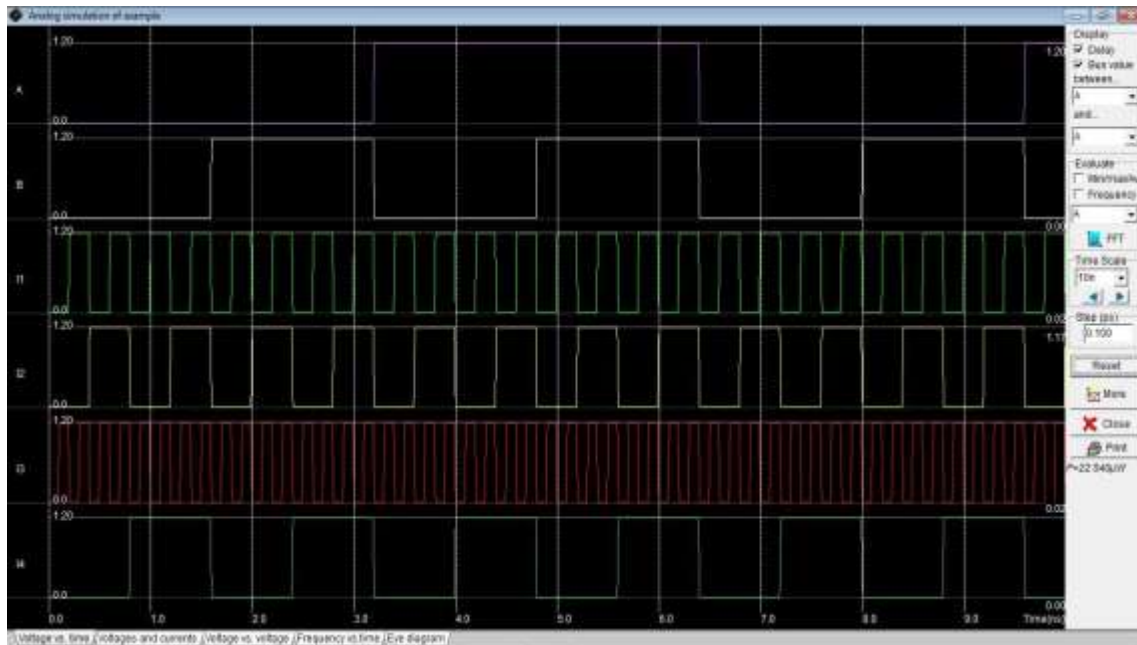


Fig 2.7: Voltage VS Time relationship in analog domain.

### III. ALU DESIGN

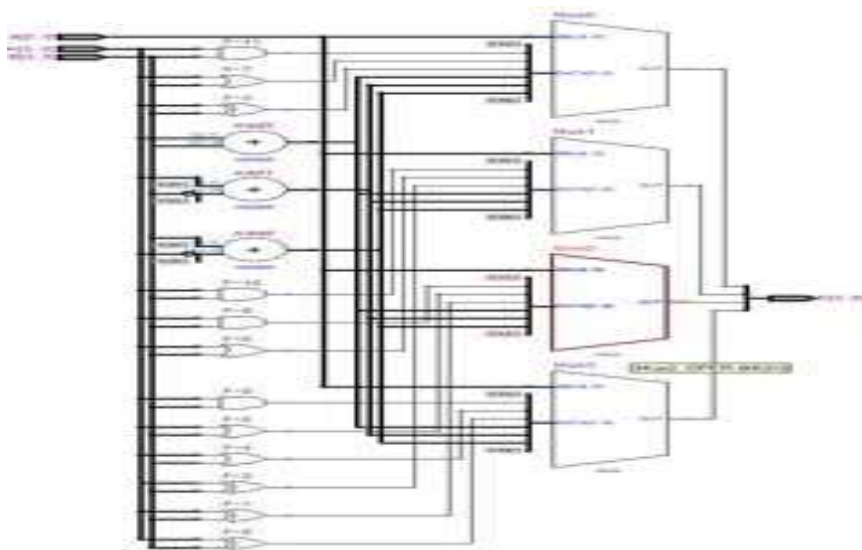


Fig3: Logical diagram of ALU

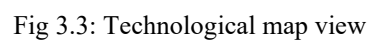
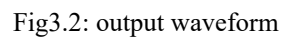
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The screenshot displays the Quartus II IDE. The main window shows the Verilog HDL code for an ALU. The code defines an ALU with inputs A, B, and a select signal 's'. It implements a 4-to-1 multiplexer logic. The Messages window at the bottom shows a warning message: "Warning: (10130) Pin 'F[3]' is 10.000 ns from being driven by 's[1]'. This is a timing violation. The message is circled in red.

Fig 3.1: VHDL Code compilation





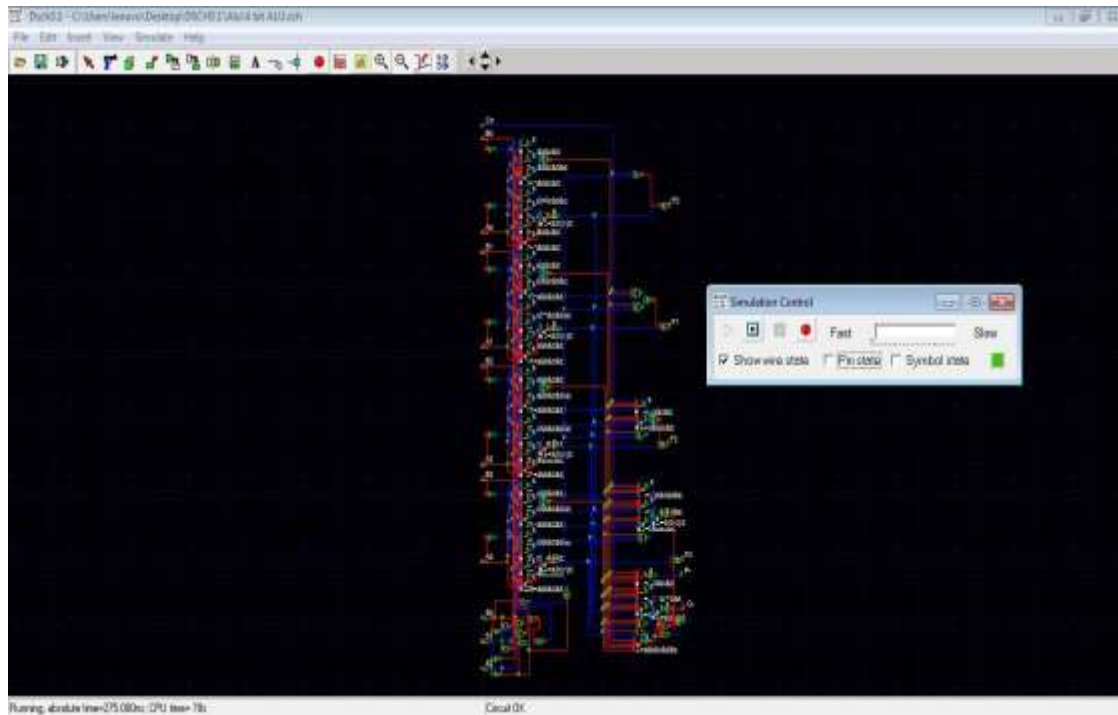


Fig 3.4: Schematic of ALU after execution in analog domain

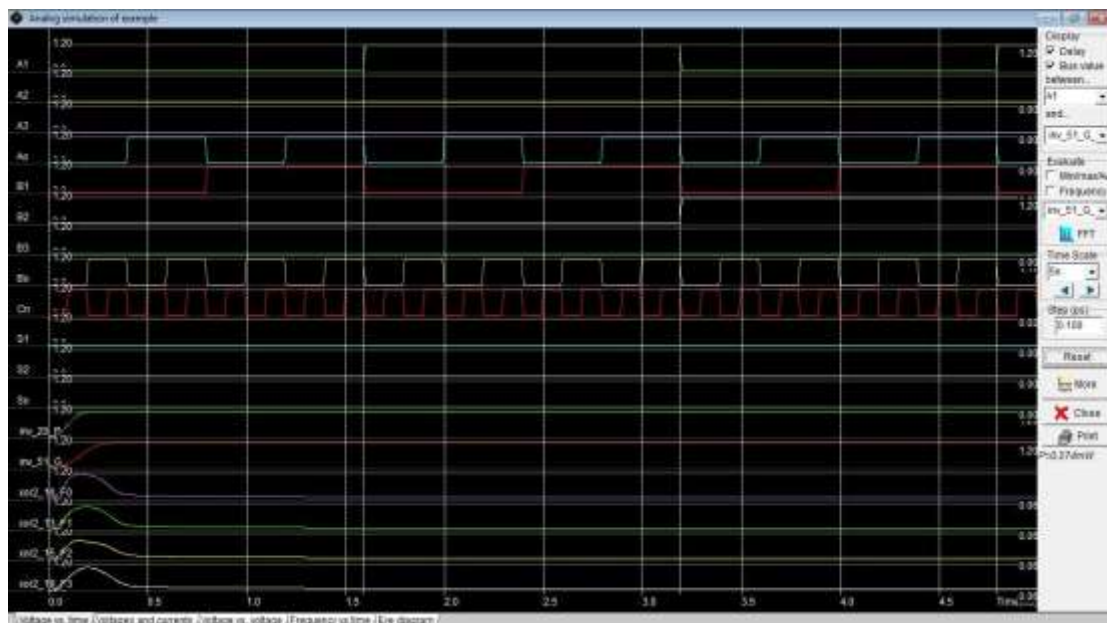


Fig 3.5: Layout of ALU circuit



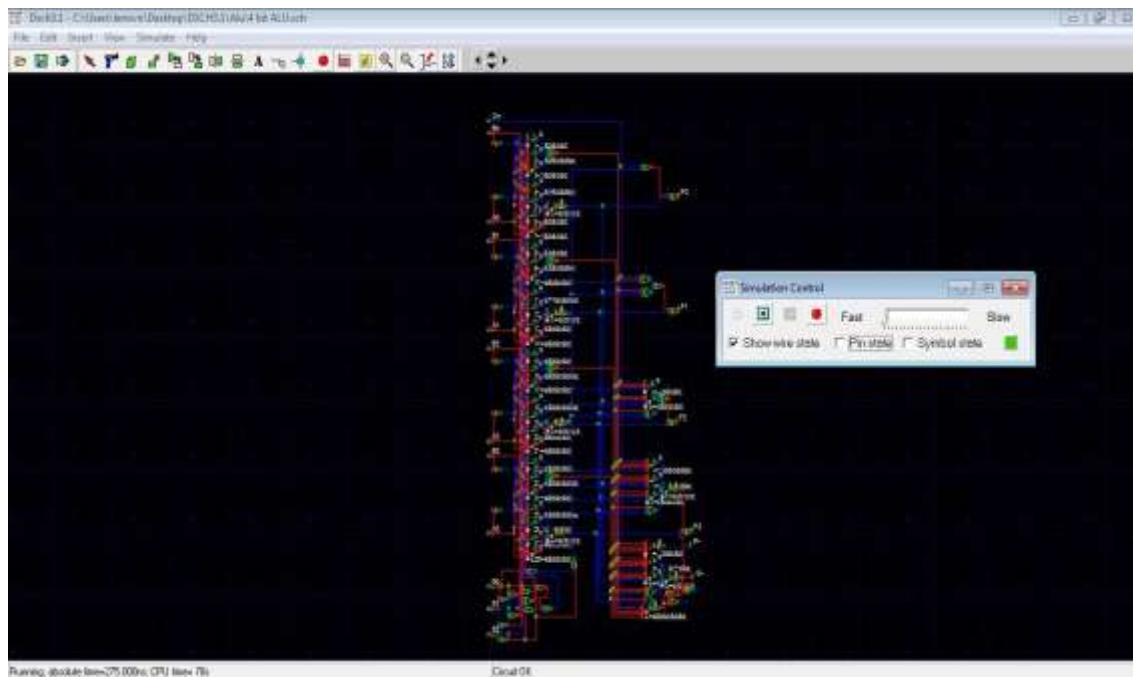


Fig 3.6: Voltage VS Time relationship in analog domain.

## RESULT ANALYSIS

From the above experimental work we can observe that designing a combinational & sequential circuit in analog domain is complicated than designing a same circuit in digital domain. If we observe carefully the design of less complex circuit in analog as well as in digital domain is not difficult, also it is easier to debug the error. but as we move on to complex circuit design e.g. ALU, it can be seen that designing in analog domain is very difficult as well as time consuming also it is very difficult to locate and debug the error if any. We are designing this project in analog and digital circuit. The main purpose of the project is to design a complex circuit in the simple form. Here we have designed combinational circuit i.e. mux or adder, this circuit is very simple to design and the time consumption is very less and it is very easy to locate and debug the error if any, and if we designing a 4 bit ALU having complex logic circuit, its design in analog domain is very complex and it is time consuming also it is difficult to locate and debug the error so to avoid this problem we have used designing in digital domain.

## CONCLUSION

CMOS 90nm model is used to design a layout of ALU and 4x1 MUX. Simulation results show successful compilations of VHDL code and its conversion into Verilog file which is used to make a layout using microwind tool. Tools used are Quartus II, Dsch & microwind. From both performance standpoint and cost standpoint, these results show that CMOS is very competitive with available technologies.

From the overall above discussion we can conclude that VHDL plays a key role in digital system design also working in digital domain or designing circuit in digital domain is more efficient, convenient and less time consuming as compared to analog domain, here in this paper we have studied the role of VHDL in digital system design also we have designed and simulated some combinational circuit to show the comparative analysis in working with analog and digital domain. The simulations are done directly using the Quartus II tool for digital domain and Dsch and Microwind tool for analog domain. There is an immense scope for further work in the field of circuit design & simulation with VHDL.



## REFERENCES

1. Rupesh Prakash Raghatate<sup>1</sup>, Swapnil S. Rajurkar<sup>2</sup>, Priyanka U Badhe<sup>3</sup>, Pravin L. Turale<sup>4</sup>, "Design and Implementation of Full Adder Using Vhdl and Its Verification in Analog Domain" International Journal of Engineering Science Invention ISSN (Online): 2319 – 6734, ISSN (Print): 2319 – 6726 www.ijesi.org Volume 2 Issue 4 | April. 2013 | PP.35-39
2. Bhaskar, J of A VHDL Primer. PHI (2012).
3. Brown, S & Rose, T. Architecture of FPGAs and CPLDs.
4. Brown, S and Vranesic, fundamentals of DIGITAL LOGIC with verilogdesign. TMH (2009).
5. Nimje, A, R, Design and Implication of some digital sequence detector network, project report M.Sc II (Ele.).
6. Pedroni, V, A, Circuit Design and Simulation with VHDL. PHI (2012)
7. Roth, C, H, Digital System Designed using VHDL, (2008).